CLAIMS

-1. A method of plating metallic material on the surface of a dielectric material, said method comprising:

-dipping the surface of the dielectric material in a solution containing catalytic metal particles which have a slight electrostatic dipole when in solution to help those particles attach to the dielectric material's surface; and

-placing the surface of the dielectric material in a metal salt solution in metastable equilibrium with a reducing agent so as to cause the metal to be plated upon the surface of the dielectric material containing the catalytic metal particles by a process of electroless plating.

-2. A method as in Claim 1 further including, before dipping the dielectric material in the solution of catalytic metal particles, plasma etching the surface of the dielectric material to roughen its surface and to create peaks and valleys in the surface of that material which have van der Waal forces capable of attracting catalytic particles which have a slight electrostatic dipole.

-3. A method as in Claim 2 wherein the plasma etching is non-reactive ion etching.

-4. A method as in Claim 1 wherein the dielectric material is latex.

-5. A method as in Claim 1 wherein the dielectric material is polyimide.

-6. A method as in Claim 1 wherein the material deposited by the electroless plating is a conductor

-7. A method as in Claim 6 wherein the deposited material is copper.

-8. A method as in Claim 1 wherein the catalytic particles are particles of one of the following metals: cobalt, palladium, ruthenium, rhodium, platinum, iridium, osmium, nickel, or iron.

-9. A method as in Claim 1 wherein the solution containing the catalytic particles contains chemicals to reduce the tendency of the catalytic particles to conglomerate in solution.

-10. A method as in Claim 1 further including using electroplating to put down an additional thickness of material on the layer of material which has been deposited by electroless plating.

-11. An electrical circuit comprised of:

-one or more dielectric layers comprised of latex; and

-one or more layers of electrically conductive material patterned to form multiple electrical interconnects, with each such layer placed on top of one of said dielectric layers.

-12. A circuit as in Claim 11 wherein the electrically conductive material is copper

-13. A circuit as in Claim 11 wherein the dielectric and conductive layers are used to connect individual bonding pads on different integrated circuits which are part of a multichip module.

-14. A circuit as in Claim 11 which has been made by a process comprising:

-dipping the surface of the dielectric material in a solution containing catalytic metal particles which have a slight electrostatic dipole when in solution to help those particles attach to the dielectric material's surface; and

-placing the surface of the dielectric material in a metal salt solution in metastable equilibrium with a reducing agent so as to cause a layer of conductive metal to be plated upon the surface of the dielectric material containing the catalytic metal particles by a process of electroless plating.

-15. A circuit as in Claim 14 wherein said process further includes, before dipping the dielectric material in the solution of catalytic metal particles, plasma etching the surface of the dielectric material to roughen its surface and to create peaks and valleys in the surface of that material which have van der Waal forces capable of attracting catalytic particles which have a slight electrostatic dipole.

-16. A circuit as in Claim 14 wherein the process used to make the circuit further includes using electroplating to put down an additional thickness of conductive material on the layer of conductive material which has been deposited by electroless plating.

-17. A multichip module comprising:

-a plurality of integrated circuits mounted on a substrate;

-one or more dielectric layers comprised of a flexible dielectric material; and

-one or more layers of electrically conductive material patterned to form multiple electrical interconnects between bonding pads on different ones of said integrated circuits, with each such layer placed on top of one of said dielectric layers.

-18. A multichip module as in Claim 17 wherein the dielectric material is latex

-19. A multichip module as in Claim 17 wherein the dielectric material is a silicon based adhesive

-20. A multichip module as in Claim 17 which has been made by a process comprising:

-dipping the surface of the dielectric material in a solution containing catalytic metal particles which have a slight electrostatic dipole when in solution to help those particles attach to the dielectric material's surface; and

-placing the surface of the dielectric material in a metal salt solution in metastable equilibrium with a reducing agent so as to cause a layer of conductive metal to be plated upon the surface of the dielectric material containing the catalytic metal particles by a process of electroless plating.

-21. A multichip module as in Claim 20 wherein said process further includes, before dipping the dielectric material in the solution of catalytic metal particles, plasma etching the surface of the dielectric material to roughen its surface and to create peaks and valleys in the surface of that material which have van der Waal forces capable of attracting catalytic particles which have a slight electrostatic dipole.

-22. A multichip module as in Claim 20 wherein the process used to make the circuit further includes using electroplating to put down an additional thickness of conductive material on the layer of conductive material which has been deposited by electroless plating.

-23. A method of manufacturing a multichip module comprising:

-placing a frame on a first flat substrate, said frame having holes in it for positioning and holding integrated circuit chips;

-placing integrated circuit chips through frame to planarize their top, active, surfaces against the first flat substrate;

-removing the first substrate from the frames and the chips;

-placing one or more layers of dielectric on top of the frames and chips;

-using photolithographic techniques to etch vias through each of the one or more dielectric layers to allow selective contact to conductive bonding pads on individual chips or conductive paths on a dielectric layer below;

-using photolithographic techniques to lay down conductive material in such vias and in desired conductive pathways on the currently to layer of dielectric material.

-24. A method as in Claim 23 further including placing a layer of adhesive dicing tape between the frame and the first flat substrate to help adhere the frame and the tops of the chips to the same planar level.

-25. A method as in Claim 23 further including placing epoxy on the back of chips and attaching the chips and frame to a second substrate on the opposite side of the frame from first substrate.

-26. A method as in Claim 25 wherein the epoxy is both thermally and electrically conducting.

-27. A method as in Claim 25 wherein the second substrate is a ball grid pad.

-28. A method as in Claim 25 wherein the second substrate has had passive components formed on it before attachment to the frame and the chips held in the frame.

-29. A method as in Claim 23 wherein the frame is made of plastic.

-30. A method as in Claim 23 wherein the dielectric material is flexible

-31. A method as in Claim 30 wherein the conductive material is a ductile conductive material.

-32. A method as in Claim 31 wherein the conductive material is copper.

-33. A method as in Claim 30 wherein the dielectric material is latex.

-34. A method as in Claim 30 wherein the dielectric material is a silicon based adhesive.

-35. A method as in Claim 23 wherein said photolithographic techniques for laying down conductive material comprising:

-dipping the surface of the dielectric material in a solution containing catalytic metal particles which have a slight electrostatic dipole when in solution to help those particles attach to the dielectric material's surface; and

-placing the surface of the dielectric material in a metal salt solution in metastable equilibrium with a reducing agent so as to cause a layer of conductive metal to be plated upon the surface of the dielectric material containing the catalytic metal particles by a process of electroless plating.

-36. A method as in Claim 35 further including, before dipping the dielectric material in the solution of catalytic metal particles, plasma etching the surface of the dielectric material to roughen its surface and to create peaks and valleys in the surface of that material which have van der Waal forces capable of attracting catalytic particles which have a slight electrostatic dipole.

-37. A method as in Claim 36 wherein the plasma etching is non-reactive ion etching.

-38. A method as in Claim 35 wherein said photolithographic techniques for laying down conductive material further include using electroplating to put down an additional thickness of conductive material on the layer of conductive material which has been deposited by electroless plating.

-39. A method of manufacturing a multichip module comprising:

-placing integrated circuit chips against a first flat substrate to planarize their top, active, surfaces against said first substrate;

-placing epoxy on the back of said chips;

-attaching the chips to a second substrate on the opposite side of the chips from the first substrate;

-removing the first substrate;

-filling space between chips with fluid filler material that can be hardened into a relatively flexible material;

-hardening said filler material;

-placing one or more additional layers of dielectric material on top of the filler material and the chips;
-using photolithographic techniques to etch vias through each of said additional dielectric layer to allow selective contact to conductive bonding pads on chips or conductive paths on dielectric layer below; and
-using photolithographic techniques to lay down conductive material in vias and in desired conductive pathways on the current top dielectric layer.

-40. A method as in Claim 39 wherein the dielectric material of said additional layers is latex.

-41. A method as in Claim 39 wherein the dielectric material of said additional layers is a silicon based adhesive.

-42. A method as in Claim 39 wherein the filler material is latex.

-43. A method as in Claim 39 wherein the filler material is a silicon based adhesive

-44. A method as in Claim 39 wherein Teflon coated pins are used to form holes in the filler material as it is hardened.